

PRODUCT / PROCESS CHANGE NOTIFICATION	
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1. PCN basic data	
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1.1 Company		STMicroelectronics International N.V
1.2 PCN No.		AMG/18/10617
1.3 Title of PCN		Linear Voltage Regulators: HBIP40 Technology Introduction for the 5V and 3.3V Output Voltage versions of the L78L Product Family
1.4 Product Category		See product list
1.5 Issue date		2018-02-09

2. PCN Team	
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2.1 Contact supplier	
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2.1.2 Phone	+1 8475853058
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2.2 Change responsibility	
2.2.1 Product Manager	Lorenzo NASO
2.1.2 Marketing Manager	Marcello SAN BIAGIO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
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3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Wafer Fab (Equipment)	New equipment changing process technique or using different technology	Front end : ST Singapore (Ang Mo Kio)

4. Description of change		
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	Old	New
4.1 Description	LAAT Technology	HBIP40 Technology
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No changes in term of Quality and Reliability. Negligible changes in the Electrical Characteristics (see Revision 26 of Datasheet).	

5. Reason / motivation for change	
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5.1 Motivation	Progressing on the activities related to a continuous improvement philosophy, a more fine Geometry Bipolar Technology called HBIP40 has been also qualified for the L78L product family. Only the 5V and 3.3V Output Voltage versions have been involved. This PCN is an extension of the PCN9952 already released in November 2016.
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change	
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6.1 Description	The traceability of the HBIP40 Technology parts will be ensured by different internal codification and QA number
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7. Timing / schedule	
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7.1 Date of qualification results	2017-12-07
7.2 Intended start of delivery	2018-05-05
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation	
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8.1 Description	10617 329-W-17- LA05 - L78L05ABZ in TO92 (Ase Weihai Subcontractor).pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2018-02-09

9. Attachments (additional documentations)

10617 Public product.pdf
10617 329-W-17- LA05 - L78L05ABZ in TO92 (Ase Weihai Subcontractor).pdf

10. Affected parts

10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
L78L33ABZ-AP	L78L33ABZ-AP	
L78L33ACZ	L78L33ACZ	

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Reliability Report

TO92 package in Ase Weihai Subcontractor

General Information		Locations	
Product Line	XL05BA6	Wafer fab	Singapore 6
Product Description	5V 100mA Pos. Reg.	Assembly plant	ASE WEIHAI
P/N	L78L05ABZ-TR	Reliability Lab	Catania Reliability LAB
Product Group	AMG	Reliability assessment	Pass
Product division	General Purpose Analog & RF POWER MANAGEMENT		
Package	TO92		
Silicon Process technology	HBiP40V		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	November 2017	7	Alfio Rao	Giovanni Presti	Final Report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the TO92 in ASE Weihai.

FE

TV1: XL05 Cr/Ni/Ag - HBIP40
Technology already validated by product

BE

TO92 in ASE Weihai

3 different qualification Lots are requested

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

L78L

Positive voltage regulators



or

The L78L series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat-sink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The L78L series used as Zener diode/resistor combination replacement, offers improvement along with lower quiescent current and lower noise.

4.2 Construction note

P/N: **L78L05ABZ-TR**

Wafer/Die fab. information	
Wafer fab manufacturing location	SINGAPORE Ang Mo Kio
Technology	HBIP40
Die finishing back side	LAPPED SILICON
Die size	766, 706 micron
Passivation type	P-VAPOX/NITRIDE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ETS300
Test program	LA05QAE01
Assembly information	
Assembly site	ASE Weihai
Package description	TO92
Molding compound	Epoxy
Frame	TO-237
Die attach material	AG EPOXY
Wires bonding materials/diameters	1.0 mils Cu
Final testing information	
Testing location	ASE Weihai
Tester	AZ400S
Test program	LA05.WOOSEOK.

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Technical Code	Package	Product Line	Part number
1				
2				
3	RWSX*LA05BA6	TO 92	XL05BA6	L78L05ABZ-TR

5.2 Test plan and results summary

P/N: **L78L05ABZ-TR**

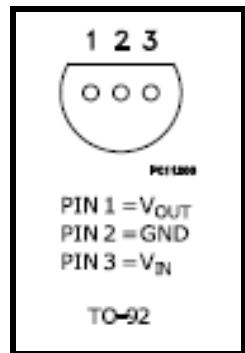
Test	Std ref.	Conditions	SS	Steps	Failure/SS			Note
					Lot 1	Lot 2	Lot 3	
Die Oriented Tests								
HTOL	JESD22 A-108	T _j = 125° C, BIAS= 30 V	77	168 h	0/ 77			
				500 h	0/ 77			
				1000 h	0/ 77			
HTSL	JESD22 A-103	Ta= 150° C	75	168 h	0/ 25	0/ 25	0/ 25	
				500 h	0/ 25	0/ 25	0/ 25	
				1000 h	0/ 25	0/ 25	0/ 25	
Package Oriented Tests								
AC	JESD22 A-102	Pa=2 Atm / Ta= 121° C	75	96 h	0/ 25	0/ 25	0/ 25	
TC	JESD22 A-104	Ta= - 65° C to 150° C	75	100 cy	0/ 25	0/ 25	0/ 25	
				200 cy	0/ 25	0/ 25	0/ 25	
				500 cy	0/ 25	0/ 25	0/ 25	
THB	JESD22 A-101	Ta= 85° C, RH= 85%, BIAS= 24 V	75	168 h	0/ 25	0/ 25	0/ 25	
				500 h	0/ 25	0/ 25	0/ 25	
				1000 h	0/ 25	0/ 25	0/ 25	
Other Tests								
ESD	JS002	CDM ESDA/JEDEC	3	±250 V	Pass			
			3	±500 V	Pass			
CA		Construction Analysis				Done		

6 ANNEXES

6.1 Device details

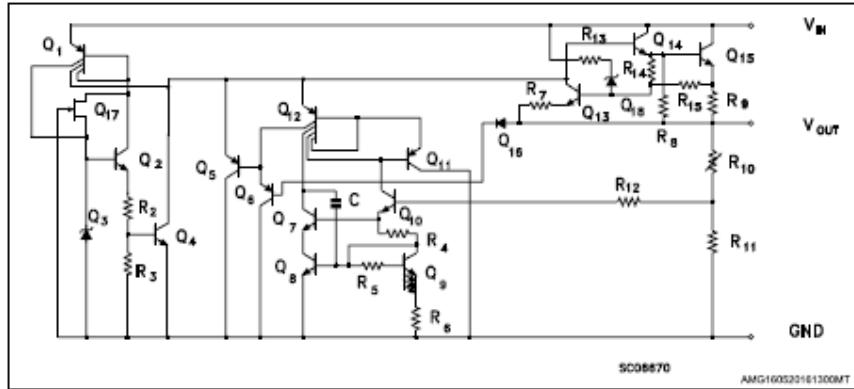
6.1.1 Pin configuration

Pin connection (bottom view for TO-92)



6.1.2 Block diagram

Schematic diagram



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
CA Construction Analysis	Construction Analysis	To verify the physical product conformity